REMARKS

The claims remaining in the present application are Claims 1-2 and 4-8. Claims 5-8 have been added. The instant specification has been amended. No new matter has been added as a result of these amendments.

ALLOWABLE SUBJECT MATTER

Claim 2 is objected to as being dependent upon a rejected base claim, but indicated as allowable if rewritten to include the limitations of the base claim. The Applicants thanks the Examiner for indicating this allowable subject matter.

SPECIFICATION

The instant specification has been amended to correct informalities. No new matter has been added as a result of these amendments.

35 U.S.C. §102

Claims 1 and 4 are rejected under 35 U.S.C. §102(b) as being anticipated by Robinson et al., U.S. Patent No. 5,307,504 (hereinafter, Robinson). The rejection to Claims 1 and 4 is respectfully traversed for the reasons below.

CLAIM 1

Claim 1 recites, in part:

> beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores,

Claim 1 recites "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores," as claimed.

Robinson fails to teach or suggest that state is immediately committed at the beginning of a speculative sequence of host instructions. Applicants assert that even if the G3 and G4 instructions taught by Robinson are interpreted as committing state, these instructions follow the G1 and G2 instructions. Thus, the G3 and G4 instructions are always the last instructions in the sequence of "y" instructions. Hence, Applicants respectfully assert that Robinson does not teach or suggest the claimed limitation of "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores."

Claim 1 further recites, "a speculative *sequence of host instructions following a branch.*" The rejection states that the Applicants' specification defines a possible meaning of speculation as, "the temporary storage of results until execution has completed successfully." Applicants do not deny

that the definition of speculation may encompass, "the temporary storage of results until execution has completed successfully." Applicants assert, however, that the definition of speculation is not limited to, "the temporary storage of results until execution has completed successfully." The Applicants further note that the claimed language uses the term "speculative" to limit the type of host instruction to those that are speculative.

The Applicants note that on page 8, line 12 of the instant specification the Applicants have disclosed, "[t]he translation and optimization software may speculate that one branch will almost always be taken and consider that direction as the normal direction of the sequence of instructions." Thus, in this case, the claim language, "a speculative sequence of host instructions following a branch," means the sequence of host instructions following a branch instruction that translation and optimization software (or the like) speculates will be executed as a result of the outcome of the branch instruction. The instruction are speculative because they are processed before the branch condition is evaluated.

Robinson is concerned with preserving granularity of "x" instructions. However, Robinson is silent as to speculating while processing a branch instruction, as claimed. Thus, Applicants do not understand Robinson to teach or suggest the claimed, "speculative sequence of host instructions following a branch," as claimed.

For the foregoing rationale, it is respectfully submitted that Claim 1 is not anticipated or rendered obvious by Robinson. As such, allowance of Claim 1 is respectfully requested.

CLAIM 4

Claim 4 recites, in part:

> translating a *first speculative sequence of host instructions* from a first sequence of target instructions from a point in the translation of target instructions at which state of the target processor is known,
>
> ending the first sequence of target instructions in response to *encountering a branch* from the first sequence in the target program by:
>
> *branching to a branch sequence of target instructions, committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions.*

For the reasons discussed in the response to the rejection to Claim 1 based on Robinson, Claim 4 is not anticipated nor rendered obvious by Robinson because Robinson fails to teach or suggest, "committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken *before executing a branch sequence of host instructions*," as claimed.

Babaian

Claims 1 and 4 are rejected under 35 U.S.C. §102(e) as being anticipated by Babaian et al., U.S. Pre-Grant Publication 2002/0,092,002 A1

(hereinafter, Babaian). The rejection to Claims 1 and 4 is respectfully traversed for the reasons set forth below.

CLAIM 1

Claim 1 recites, in part:

> beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores,

Babaian was filed on April 18, 2001, which is after the filing date of the present Application. Babaian is a continuation in part of U.S. Patent Application No. 09/505,652, filed on February 17, 2000 (also filed after the filing date of the present application). Thus, the Babaian reference may contain new matter not disclosed in U.S. Patent Application No. 09/505,652. United States Patent Application No. 09/505,652 claims priority to several provisional applications that were filed in the United States Patent and Trademark Office on February 17, 1999.

Applicants respectfully assert that if Babaian is to be used as a 35 U.S.C. §102(e) against the present application, that the rejection must demonstrate that at least one of the affore-mentioned provisional patent applications filed on February 17, 1999 contains support under 35 U.S.C §112 for the subject matter in Babaian that the rejection has cited against embodiments of the present invention.

Applicants further traverse the rejection on the grounds that Babaian fails to teach or suggest, "a speculative sequence of host instructions following a branch," as claimed. In light of the remarks Applicants have made in the response to the rejection based on Robinson, Applicants respectfully assert that Babaian's teaching of a "speculative mode" in which values are temporarily stored fails to teach or suggest, "a speculative sequence of host instructions following a branch," as claimed.

CLAIM 4

Claim 4 recites, in part:

> translating a *first speculative sequence of host instructions* from a first sequence of target instructions from a point in the translation of target instructions at which state of the target processor is known,
>
> ending the first sequence of target instructions in response to encountering a branch from the first sequence in the target program by:
>
> *branching to a branch sequence of target instructions, committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions.*

For the reasons discussed in the response to the rejection of Claim 1 based on Babaian, Claim 4 is not anticipated nor rendered obvious by Babaian because Babaian fails to teach or suggest, "committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions," as claimed

Kelly

Claims 1 and 4 are rejected under 35 U.S.C. §102(e) as being anticipated by Kelly et al., U.S. Patent No. 5,958,061 (hereinafter, Kelly). The rejection to Claims 1 and 4 is respectfully traversed for the reasons below.

CLAIM 1

Claim 1 recites, in part:

> beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores,

Kelly fails to teach or suggest, "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores," as claimed. Kelly may teach that a commit operation is performed after a sequence of host instructions executes without an exception occurring. For example, Kelly at col. 12, line 58 et seq. may disclose that a commit occurs after one or a group of target instructions has been translated and run without error. However, Kelly is silent as to, "beginning execution of a speculative sequence of host instructions following a branch from the first sequence of target instructions by immediately committing state and storing memory stores," as claimed. For example, Kelly does not disclose that the commit occurs before a speculative sequence of host instructions that follows a branch, as claimed.

CLAIM 4

Claim 4 recites, in part:

> translating a first speculative sequence of host instructions from a first sequence of target instructions from a point in the translation or target instructions at which state of the target processor is known...
>
> committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions.

For the reasons discussed in the response to the rejection of Claim 1 based on Kelly, Claim 4 is neither anticipated nor rendered obvious by Kelly because Kelly fails to teach or suggest, "committing state of the target processor and storing memory stores generated by the first translation sequence after a branch taken before executing a branch sequence of host instructions," as claimed.

For the foregoing rationale, Claims 1 and 4 are neither taught nor suggested by Robinson, Babaian, or Kelly. Therefore, Applicants respectfully solicit the allowance of Claims 1 and 4.

NEW CLAIMS

Claims 5 - 8 have been added. Support for new Claim 5 may be found at least in Claim 3, as filed. Support for new Claim 6 may be found in the instant

specification at least at page 12, line 8 - page 13, line 13. Support for new Claim 7 may be found at least at page 7, line 11 - page 12, line 7. Support for new Claim 8 may be found in the instant specification at least at page 13, line 14 - page 14, line 6. No new matter has been added as a result of the additional claims.

Claim 5 recites, in part:

> executing a sequence of host instructions from the first sequence of target instructions commencing immediately after committing state of the target processor and storing memory stores previously generated by execution until another point in the translation of target instructions at which state of the target processor is known.

Applicants respectfully assert that the prior art fails to teach or suggest, "executing a sequence of host instructions from the first sequence of target instructions commencing immediately after committing state of the target processor and storing memory stores previously generated by execution."

Claim 6 is respectfully believed to be allowable at least based on its dependency from Claim 5, which is respectfully believed to be allowable for foregoing reasons.

Claim 7 recites, in part:

> speculating that execution of a branch instruction will cause a branch to a first sequence of host instructions;
> committing state of the target processor and storing memory stores from previously executed host instructions after the branch instruction is executed and prior to beginning execution of the first sequence of host instructions.

Applicants respectfully assert that the prior art fails to teach or suggest speculating that execution of a branch instruction will cause a branch to a first sequence of host instructions and committing state of the target processor and storing memory stores from previously executed host instructions after the branch instruction is executed and prior to beginning execution of the first sequence of host instructions.

Claim 8 recites, in part:

> if a sequence of instructions includes a locking operation, placing a commit operation at the beginning of the sequence of instructions including the locking operation; and
> if a sequence of instructions does not include a locking operation, placing a commit operation at the end of the sequence of instructions not including the locking operation.

Applicants respectfully assert that the prior art fails to teach or suggest if a sequence of instructions includes a locking operation, placing a commit operation at the beginning of the sequence of instructions including the locking operation; and if a sequence of instructions does not include a locking operation, placing a commit operation at the end of the sequence of instructions not including the locking operation.

CONCLUSION

In light of the above listed amendments and remarks, reconsideration of the rejected Claims is requested. Based on the arguments and amendments presented above, it is respectfully submitted that Claims 1-2 and 4-8 overcome the rejections of record and, therefore, allowance of Claims 1-2 and 4-8 is earnestly solicited.

Should the Examiner have a question regarding the instant response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
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Dated: 5/5, 2004

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